In the Claims

(Original) A memory controller, comprising:

means to detect a first start address for a first burst output from a memory cell array; and

means to generate an anticipated start address for an anticipated burst output, wherein the anticipated start address is based on the first start address and is in anticipation of a second start address such that, when the anticipated start address corresponds to the second start address, the anticipated burst output follows the first burst output and maintains an active data output stream from the memory cell array for the first burst output associated with the first start address and a second burst output associated with the second start address.

2.   (Original) The memory controller of claim 1, wherein the means to provide an anticipated start address includes means to advance one or more most significant bits (MSB's) of the first start address to provide the anticipated start address.

3.   (Original) The memory controller of claim 1, further comprising means to compare the second start address to the anticipated start address to determine whether the anticipated burst output corresponds to the second burst output.

4.   (Original) A memory controller, comprising:

means to provide a first burst output from a memory cell array in response to a first start address from a microprocessor;

means to provide an anticipated start address in anticipation of a second start address from the microprocessor; and

means to initiate an anticipated burst output from the memory cell array in response to the anticipated start address, wherein the anticipated burst output follows the first burst output and maintains an active data output stream from the memory cell array for the first start address and the second start address.

5.   (Original) The memory controller of claim 4, further comprising means to compare the anticipated start address to the second start address from the microprocessor to determine whether the anticipated burst output corresponds to a desired second burst output from the memory cell array that corresponds to the second start address from the microprocessor.

6.   (Original) The memory controller of claim 4, wherein the means to provide an anticipated start address includes means to advance one or more most significant bits (MSB's) of the first start address to provide the anticipated start address.

7.   (Original) The memory controller of claim 4, further comprising means to generate a linear sequence of addresses for the first burst output and the anticipated burst output.

8.   (Original) The memory controller of claim 4, further comprising means to generate an interleaved sequence of addresses for the first burst output and the anticipated burst output.

9.   (Original) A system, comprising:

        a burst access memory, the burst access memory to provide a first burst read output in response to a first memory address; and

        an address generator to initiate an anticipated burst read output from the burst access memory beginning with an anticipated memory address;

        wherein, when the anticipated memory address corresponds to a second start address and the anticipated burst read output corresponds to a second burst read output beginning with the second start address, the second burst read output follows the first burst read output and maintains an active data output stream from the burst access memory for the first start address and the second start address.

10.   (Original) The system of claim 9, further comprising a memory controller to communicate with the burst access memory, the memory controller including the address generator.

11.   (Original) The system of claim 10, wherein the memory controller further includes a comparator to compare the anticipated start address to the second start address.

12.   (Original) The system of claim 9, wherein the burst access memory includes the address generator.

13.   (Original) The system of claim 9, further comprising a comparator to compare the anticipated start address to the second start address.

14.   (Original) A system, comprising:

a burst access memory;

a processor to request a first read operation followed by a second read operation, the processor to provide a first start address to the burst access memory for the first read operation and to provide a second start address to the burst access memory for the second read operation;

an address generator to detect the first start address and provide an anticipated start address to the burst access memory in response to the first start address;

the burst access memory to output a first burst output in response to the first start address and to output an anticipated burst output in response to the anticipated start address,

wherein, when the anticipated start address corresponds to the second start address, the anticipated burst output follows the first burst output and maintains an active data output stream from the burst access memory from the first read operation to the second read operation.

15.   (Currently Amended) The system of claim 14, wherein the address generator is adapted to advance one or more most significant bits (MSB's) of the first start address to provide the anticipated start address.

16.   (Original) The system of claim 14, wherein the burst access memory includes the address generator.

17.   (Original) The system of claim 14, further comprising a memory controller to
communicate with the burst access memory, the memory controller including the address
generator.

18.   (Original) A system, comprising:

        addressable memory cells;

        a processor to generate a first start address to read the memory cells; and

        a memory controller to receive the first start address, to output a first data series from the
addressable memory cells to the processor in response to receiving the first start address, to
generate an anticipated start address in response to receiving the first start address, and to output
an anticipated data series from the addressable memory cells such that the anticipated data series
follows the first data series to maintain an active data output stream from the addressable
memory cells to the processor.

19.   (Currently Amended) The system of claim 18, wherein the memory controller to advance
one or more most significant bits (MSB's) of the first start address to provide the anticipated start
address.

20.   (Currently Amended) The system of claim 18, wherein the memory controller is adapted
to generate a linear sequence of addresses for the first data series and the anticipated data series.

21.   (Currently Amended) The system of claim 18, wherein the memory controller is adapted
to generate an interleaved sequence of addresses for the first data series and the anticipated data
series.

22.   (Currently Amended) The system of claim 18, wherein the processor is adapted to
generate a second start address and the memory controller is adapted to compare the second start
address to the anticipated start address.

23.   (Currently Amended) The system of claim 18, wherein the memory controller is adapted

to provide the anticipated start address to the processor for comparison to a second start address.

24.   (Original) A system, comprising:

a memory device, including addressable memory cells and control circuitry to provide

burst outputs from the addressable memory cells in response to an address;

a processor to request a first burst read operation from the addressable memory cells

followed by a second burst read operation from the addressable memory cells, the processor to

provide a first address to the control circuitry of the memory device for the first burst read

operation and to provide a second address to the control circuitry of the memory device for the

second burst read operation, the memory device to output a first burst output in response to the

first address; and

an address generator to provide an anticipated address to the memory device based on the

first address such that the memory device outputs an anticipated burst output, wherein when the

anticipated address corresponds to the second address, the memory device maintains an active

data stream for the first burst read operation and the second burst read operation.

25.   (Original) The system of claim 24, further comprising a memory controller to

communicate with the memory device, the memory controller including the address generator.

26.   (Original) The system of claim 24, wherein the memory device includes an address

generator.

27.   (Currently Amended) The system of claim 24, wherein the address generator is adapted

to advance one or more most significant bits (MSB's) of the first start address to provide the

anticipated start address.

28.   (Original) A method for outputting data from a burst access memory, comprising:

receiving a first read request, including receiving a first start address;

in response to receiving the first start address,

outputting a first data series from the burst access memory beginning

with the first start address, and

outputting an anticipated data series from the burst access memory

beginning with an anticipated start address such that the

anticipated data series follows the first data series and maintains

an active data stream from the burst access memory;

comparing a second start address to the anticipated start address;

interrupting the anticipated data series and outputting a second data series from the burst

access memory that corresponds to the second start address when the second start address does

not correspond to the anticipated start address, and outputting the anticipated data series as the

second data series when the second start address corresponds to the anticipated start address.

29.   (Currently Amended) The method of claim 28, wherein both outputting a first data series

and outputting an anticipated data series includes outputting a full column data sequence.

30.   (Original) The method of claim 28, further comprising generating the anticipated start

address using an interleaved sequence.

31.   (Currently Amended) The method of claim 28, further comprising generating the

anticipated start address using [[an]] a linear sequence.

32.   (Original) The method of claim 28, further comprising receiving the second start address,

and ignoring the received second start address when the anticipated start address corresponds to

the received second start address.

33.   (Original) The method of claim 28, further comprising sending the anticipated start

address to a processor that is sending the first and second start address such that the processor

withholds sending the second start address when the second start address corresponds to the

anticipated start address.

34.   (Original) A method for outputting data from a burst access memory, comprising:

receiving a first read request, including receiving a first start address;

in response to receiving the first start address,

outputting a first data series from the burst access memory beginning

with the first start address, and

outputting an anticipated data series from the burst access memory

beginning with an anticipated start address such that the

anticipated data series follows the first data series and maintains

an active data stream from the burst access memory;

comparing a second start address to the anticipated start address;

interrupting the anticipated data series if the second start address is not received before

the burst access memory is ready to output a second data series, the second data series

corresponding to the second start address and further corresponding to the anticipated data series

when the second start address corresponds to the anticipated start address.

35.   (Original) A method for outputting data from a burst access memory, comprising:

receiving a first read request, including receiving a first start address;

in response to receiving the first start address,

outputting a first data series from the burst access memory beginning

with the first start address, and

outputting an anticipated data series from the burst access memory

beginning with an anticipated start address such that the

anticipated data series follows the first data series and maintains

an active data stream from the burst access memory;

comparing a second start address to the anticipated start address;

interrupting the anticipated data series if the second start address is not received before a

second data series is ready to be presented to a processor, the second data series corresponding to

the second start address and further corresponding to the anticipated data series when the second

start address corresponds to the anticipated start address.

36.   (Original) A method for performing burst read operations, comprising:

receiving a first address for a first burst read operation;

in response to receiving the first address, providing a first burst output from a memory array corresponding to the first burst read operation, generating an anticipated address, and providing an anticipated burst output from the memory array following the first burst output, wherein an active data stream is maintained between the first burst output and the anticipated burst output;

comparing a second address corresponding to a second burst read operation to the anticipated address, and when the second address corresponds to the anticipated address, continuing the anticipated burst output as a second burst output from the memory array corresponding to the second burst read operation, wherein an active data stream is maintained from the first and second burst read operations.

37.   (Original) The method of claim 36, wherein comparing a second address corresponding to a second burst read operation to the anticipated address includes using a comparator in a memory controller to compare the second address to the anticipated address, and ignoring the second address when the second address corresponds to the anticipated address.

38.   (Original) The method of claim 36, wherein comparing a second address corresponding to a second burst read operation to the anticipated address includes communicating the anticipated start address to a processor that sends the first address and the second burst read operation by sending the second address, the processor to withhold the second address when the second address corresponds to the anticipated address.

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Conclusion

Claims 15, 18-23, 27, 29, and 31 are amended for clarity. It is respectfully submitted that these changes do not introduce new matter, and the claims are allowable without further search or consideration. Therefore, entry is appropriate under Rule 312, and is respectfully requested.
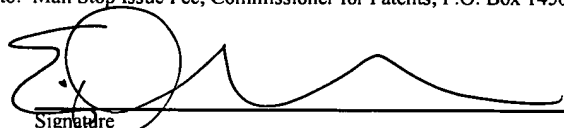
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 27 day of September, 2005.

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